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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,098	03/29/2001	Thomas D. Fletcher	42390P9006	8394

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EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,098	FLETCHER ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-11,18-21,31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-5,7,9-11,31 and 35-38* is/are allowed.

6)☒ Claim(s) *18-21* is/are rejected.

7)☒ Claim(s) *8 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicants' amendment filed on 6/24/03 has been received and entered in the case. Claims 2-5, 7-11, 18-21 and 31-38 are pending. The prior art rejections to claims 18-21 are maintained for the reasons set forth below. This action is FINAL.

Claim Objections

2. Claims 8 and 33-34 are objected to because of the following informalities:

In claim 8, line 11, -- for multiplying the frequency of the distributed global clock signal before feeding the multiplied clock signal to the duty cycle correction circuit -- should be inserted after "duty cycle correction circuit" to clearly indicate that the duty cycle correction circuit is for correcting the signal output from the frequency multiplying circuit to avoid potential 112, second paragraph problem since it does not make sense to recite both the duty cycle correction circuit and the frequency multiplying circuit coupled to a receiving point.

In claim 33, line 1, "each of" should be deleted, see claim 32, line 2, "a reset path".

In claim 34, lines 2-3, "an output signal from the duty cycle correction circuit" should be deleted since it does not make sense for this phrase to be there.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,122,679, issued to Ishii et al.

As per claim 18, Ishii discloses an integrated circuit chip (Fig. 1, LSI chip A) comprising:

a clock generation circuit (the clock generator 1) to provide a first clock signal (the master clock signal) having a first duty cycle;

a clock distribution network (all the lines from the clock generator 1) coupled to the clock generation circuit 1 to distribute the first clock signal MCK across the integrated circuit chip A; and

a plurality of duty cycle correction circuits (the circuits 2) at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of distributed first clock signals at the receiving points.

As per claim 19, the recited frequency multiplying circuit reads on the frequency divider 22 shown in Fig. 2.

As per claim 20, since the master clock has a duty cycle of 50% (Fig. 4), the corrected clock signal also has a duty cycle of 50%.

As per claim 21, the recited smart buffer reads on the phase comparator circuit 23.

Response to Arguments

4. Applicant's arguments filed 6/24/03 have been fully considered but they are not persuasive.

Regarding the argument that Ishii does not teach a duty cycle correction circuit, instead, Ishii teaches a clock skew adjuster circuit.

Ishii explicitly teaches in column 3, lines 1-4 that "each clock skew adjuster 2 is constructed to include: variable delay means 21 capable of *delaying an input signal such as the master clock MCK by an arbitrary time within one clock period*". The teaching clearly indicates that the Ishii's clock skew adjuster circuit performs the duty cycle correction function which adjusting the input signal within one clock period.

Allowable Subject Matter

5. Claims 2-5, 7-11 and 31-38 are allowed after claims 8 and 33-34 are amendment to overcome the objections noted herein above.

Claims 2-5, 7-11 and 31-38 are allowed because the prior art of record fails to disclose or suggest an apparatus which includes a frequency multiplying circuit for receiving a distributed clock signal and a duty cycle correction circuit for receiving the clock signal output from the frequency multiplying circuit, correcting the duty cycle of the received clock signal and providing a duty cycle corrected output clock signal as recited in claims 4 and 8. The Ishii's apparatus taught in Fig. 1 appears to teach the opposite which is to adjust the duty cycle of the clock signal first before multiplying the frequency of the duty corrected output clock signal.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

9/2/03

Minh Nguyen
Primary Examiner
Art Unit 2816